In the Specification

Please amend paragraph 19 as follows:

FIG. 2 illustrates a schematic of the loop filter circuit 2 in relation to the main charge pump circuit 5 and the auxiliary charge pump circuit 8, in accordance with embodiments of the present invention. The loop filter circuit 2 comprises a first capacitor 4, a second capacitor 18 (e.g., filter capacitor), and a resistor 12. The first capacitor 4 is electrically connected to the resistor 12. The resistor 12 is electrically connected to the second capacitor 18. The first capacitor 4 is in parallel with the resistor 12 and the second capacitor 18. The resistor 12 comprises a fixed resistance R1. The first capacitor 4 comprises a fixed capacitance C1. The second capacitor 18 comprises a fixed capacitance C2. The main charge pump circuit 5 may inject (i.e., source) current to the loop filter circuit 2. Alternatively, the main charge pump circuit 5 may remove (i.e., sink) current from the loop filter circuit 2. The source or sink function of the main charge pump circuit 5 may be controlled by a user. The auxiliary charge pump circuit 8 is electrically connected to the loop filter circuit 2 in parallel with the second capacitor 18. The auxiliary charge pump circuit 8 may inject (i.e., source) current to the second capacitor 18. Alternatively, the auxiliary charge pump circuit 8 may remove (i.e., sink) current from the 2 second capacitor 18. The source or sink function of the auxiliary charge pump circuit 8 may be controlled by the user. The main charge pump circuit 5 may comprise an adjustable gain control 7 so that the user may vary a current gain of the main charge pump circuit 5 (Gm). The auxiliary charge pump circuit 8 may comprise an adjustable gain control 9 so that the user may vary a current gain of the main charge pump circuit 5 (Ga). By changing the current gain Ga of the auxiliary charge pump circuit 8 in relation to the current gain Gmof the main charge pump circuit

5, an effective capacitance value of the second capacitor 18 (Ceff) may be controlled. The effective capacitance value Ceff is a value of capacitance that the [[the]] second capacitor 18 appears to have. Although the second capacitor 18 comprises the fixed capacitance value C2, the effective capacitance Ceff value is higher or lower than the fixed capacitance value C2. By changing both gains Ga and Gm relative to each other, a wide range of effective capacitance values Ceff for the second capacitor 18 is obtained. When the main charge pump circuit 5 and the auxiliary charge pump circuit 8 both flow current in a same direction (i.e., the main charge pump circuit 5 and the auxiliary charge pump circuit 8 both sink current or both source current), a value for Ceff is determined by the following first equation: Ceff = (C2* Gm)/(Gm+Ga). Using the first equation, Ceff decreases as Ga increases. When the main charge pump circuit 5 and the auxiliary charge pump circuit 8 each flow current in opposite directions (i.e., the main charge pump circuit 5 sinks current and the auxiliary charge pump circuit 8 sources current or vice versa), a value for Ceff is determined by the following second equation: Ceff = (C2* Gm)/(Gm-Ga) with a limitation that Ga< Gm. Using the second equation, Ceff increases as Ga increases. It is readily apparent that if both Gm and Ga are varied, then Ceff can be varied over a wider range then if just Gm or Ga is varied. For example, if Gm = 1, Ga = .5, and C2 = 350 picofarads (pF) then using the first equation produces a Ceff of 233pF and using the second equation produces a Ceff of 700pF thereby giving Ceff a range of 233pF-700pF. The variation of Ceff allows for optimization of phase lock loop circuit 1 parameters such as, inter alia, bandwidth, peaking/damping factor (ζ), noise reduction, etc. A relationship between the damping factor ζ and Ceff and is shown by the following equation: